THE INVENTION CLAIMED IS:

1. A method for forming an alignment mark structure using standard process steps for forming a vertical gate transistor, comprising the steps of:

forming a deep trench stud in an alignment mark region concurrently with a formation of a vertical gate transistor electrode in a circuit region;

etching the stud to reduce a top area of the stud and forming an isolation trench in the alignment mark region adjacent to the stud, both concurrently with a formation of an isolation trench adjacent to the vertical gate transistor electrode in the circuit region;

filling the alignment mark isolation trench with an insulating material while filling the circuit region isolation trenches with the insulating material; and

removing a portion of the insulating material from the alignment mark isolation trench to a level below the top of the stud so that an upper portion of the stud extends above the insulating material, concurrently with a removal of a portion of the insulating material from the circuit region isolation trenches.

2. The method of claim 1, further comprising the steps of:

forming an etch stop layer over the alignment mark region, concurrently with a formation of the etch stop layer over at least part of the circuit region; and

shielding the stud from being etched during a subsequent etch, and retaining the stud during the subsequent etch.

3. The method of claim 2, wherein the etch stop layer comprises a support gate oxide layer for planar devices in a support area of the circuit region.

4. The method of claim 2, further comprising the step of:

removing the etch stop layer from the alignment mark structure concurrently with a removal of at least part of the etch stop layer from the circuit region.

5. The method of claim 4, further comprising the step of:

after the removing etch stop layer step, removing another portion of the insulating material from the alignment mark isolation trench to another level further below the top of the

stud, concurrently with a removal of another portion of insulating material from the circuit region, such that the stud extends further above the insulating material of the alignment mark isolation trench.

6. The method of claim 2, wherein the subsequent etch is performed to remove at least a portion of a support polysilicon layer formed for building a gate electrode on a planar transistor device in a support area of the circuit region.

7. The method of claim 1, further comprising the steps of:

forming an etch stop layer over the alignment mark region, concurrently with a formation of the etch stop layer over at least part of the circuit region;

forming a layer of polysilicon over the alignment mark region, concurrently with a formation of the polysilicon layer over at least part of the circuit region;

removing the polysilicon layer at the alignment mark region, concurrently with an etch of at least part of the polysilicon layer at the circuit region;

shielding the stud from being etched and retaining the stud during the step of etching the polysilicon layer;

forming a layer of top oxide over the alignment mark region, concurrently with a formation of the top oxide layer over at least part of the circuit region; and

removing the top oxide layer at the alignment mark region, concurrently with an etch of at least part of the top oxide layer at the circuit region, to a level below the top of the stud.

8. The method of claim 7, further comprising the step of:

forming an opaque material layer over the alignment mark region, concurrently with a formation of the opaque material layer over at least part of the circuit region.

9. The method of claim 8, wherein the opaque material layer comprises metal.

10. The method of claim 7, further comprising the step of:

removing the etch stop layer from the alignment mark structure concurrently with an etch of the circuit region.

11. The method of claim 10, further comprising the step of:

forming an opaque material layer over the alignment mark region, concurrently with a formation of the opaque material layer over at least part of the circuit region.

12. The method of claim 10, further comprising the steps of:

removing another portion of the insulating material from the alignment mark isolation trench to another level further below the top of the stud, concurrently with an etch of the circuit region; and

forming an opaque material layer over the alignment mark region, concurrently with a formation of the opaque material layer over at least part of the circuit region.

13. The method of claim 2, wherein the etch stop layer comprises a nitride material.

14. The method of claim 1, further comprising the steps of:

forming a first etch stop layer over the alignment mark region, concurrently with a formation of the first etch stop layer over at least part of the circuit region;

forming a layer of top oxide over the alignment mark region, concurrently with a formation of the top oxide layer over at least part of the circuit region;

removing the top oxide layer at the alignment mark region, concurrently with a removal of at least part of the top oxide layer at the circuit region; and

shielding the structures under the first etch stop layer from being removed during the step of removing the top oxide layer.

15. The method of claim 14, further comprising the step of:

removing the first etch stop layer at the alignment mark region, concurrently with a removal of at least part of the first etch stop layer at the circuit region.

16. The method of claim 15, further comprising the step of:

forming a second etch stop layer over the alignment mark region, concurrently with a formation of the second etch stop layer over at least part of the circuit region;

forming a layer of polysilicon over the alignment mark region, concurrently with a formation of the polysilicon layer over at least part of the circuit region;

removing the polysilicon layer at the alignment mark region, concurrently with a removal of at least part of the polysilicon layer at the circuit region; and

shielding the structures under the second etch stop layer from being removed during the step of removing the polysilicon layer.

17. The method of claim 16, further comprising the step of:

forming an opaque material layer over the alignment mark region, concurrently with a formation of the opaque material layer over at least part of the circuit region.

18. The method of claim 16, further comprising the steps of:

removing the second etch stop layer at the alignment mark region, concurrently with a removal of at least part of the second etch stop layer at the circuit region; and

forming an opaque material layer over the alignment mark region, concurrently with a formation of the opaque material layer over at least part of the circuit region.

19. The method of claim 1, further comprising the steps of:

forming a layer of polysilicon over the alignment mark region, concurrently with a formation of the polysilicon layer over at least part of the circuit region; and

forming an opaque material layer over the alignment mark region, concurrently with a formation of the opaque material layer over at least part of the circuit region.

20. The method of claim 1, further comprising the steps of:

forming a layer of top oxide over the alignment mark region, concurrently with a formation of the top oxide layer over at least part of the circuit region; and

removing the top oxide layer at the alignment mark region, concurrently with a removal of at least part of the top oxide layer at the circuit region.

21. The method of claim 20, further comprising the step of:

removing another portion of the insulating material from the alignment mark isolation trench to another level further below the top of the stud, concurrently with a removal of material from the circuit region, such that the stud extends further above the insulating material of the alignment mark isolation trench.

22. The method of claim 20, further comprising the steps of:

forming an etch stop layer over the alignment mark region, concurrently with a formation of the etch stop layer over at least part of the circuit region;

forming a layer of polysilicon over the alignment mark region, concurrently with a formation of the polysilicon layer over at least part of the circuit region;

removing the polysilicon layer at the alignment mark region, concurrently with a removal of at least part of the polysilicon layer at the circuit region; and

shielding the structures under the etch stop layer from being removed during the step of removing the polysilicon layer.

23. The method of claim 22, further comprising the step of:

forming an opaque material layer over the alignment mark region, concurrently with a formation of the opaque material layer over at least part of the circuit region.

24. The method of claim 22, further comprising the steps of:

removing the etch stop layer at the alignment mark region, concurrently with a removal of at least part of the etch stop layer at the circuit region; and

forming an opaque material layer over the alignment mark region, concurrently with a formation of the opaque material layer over at least part of the circuit region.

25. The method of claim 1, wherein the alignment mark region is located in a kerf region of a wafer.

26. The method of claim 1, wherein the alignment mark region is located in the circuit region.

27. The method of claim 26, wherein the alignment mark structure is also part of an electrical component being formed in the circuit region.

28. An alignment mark structure produced by the method of claim 1.

29. An alignment mark structure produced by the method of claim 8.

30. An alignment mark structure produced by the method of claim 12.

31. An alignment mark structure produced by the method of claim 17.

32. An alignment mark structure produced by the method of claim 19.

33. An alignment mark structure produced by the method of claim 23.

34. A method for forming an alignment mark structure using standard process steps for forming a vertical gate transistor, comprising the step of:

forming a deep trench stud that extends above an adjacent surface in an alignment mark region, concurrently with a formation of a vertical gate transistor electrode in a circuit region.

35. The method of claim 34, further comprising the step of:

removing a nitride layer adjacent the stud in the alignment mark region, concurrently with the removal of at least part of the nitride layer in the circuit region.

36. The method of claim 35, further comprising the steps of:

forming an oxide layer over the alignment mark region, concurrently with the formation of the oxide layer over at least part of the circuit region; and

removing the oxide layer in the alignment mark region, concurrently with the removal of at least part of the oxide layer in the circuit region.

37. The method of claim 36, further comprising the steps of:

forming an etch stop layer over the alignment mark region, concurrently with the formation of the etch stop layer in the circuit region;

forming a polysilicon layer over the alignment mark region, concurrently with the formation of the polysilicon layer over at least part of the circuit region; and

removing the polysilicon layer in the alignment mark region, concurrently with the removal of at least part of the polysilicon layer in the circuit region.

38. An alignment mark structure produced by the method of claim 34.

39. An alignment mark structure produced by the method of claim 37.

40. A method for aligning a mask with prior formed structures in an active area of a circuit region when an alignment mark region is covered by an opaque material layer, the method comprising the steps of:

forming an alignment mark structure in the alignment mark region using standard process steps for forming a vertical gate transistor, the forming alignment mark structure step comprising the steps of:

forming a deep trench stud in an alignment mark region concurrently with a formation of a vertical gate transistor electrode in a circuit region,

etching the stud to reduce a top area of the stud and forming an isolation trench in the alignment mark region adjacent to the stud, both concurrently with a formation of an isolation trench adjacent to the vertical gate transistor electrode in the circuit region,

filling the alignment mark isolation trench with an insulating material while filling the circuit region isolation trenches with the insulating material, and

removing a portion of the insulating material from the alignment mark isolation trench to a level below the top of the stud so that an upper portion of the stud extends above the insulating material, concurrently with a removal of a portion of the insulating material from the circuit region;

forming the opaque material layer over the alignment mark region, concurrently with a formation of the opaque material layer over at least part of the circuit region;

viewing the alignment mark structure through the mask, wherein a step feature formed by the stud is still present after the opaque material layer covers the alignment mark structure; and

aligning an alignment mark portion of the mask with the alignment mark structure.

41. The method of claim 40, wherein the mask is a gate conductor mask, and wherein the opaque material layer comprises a gate conductor material.

42. An alignment mark structure for aligning a mask with prior formed features of in a circuit region when an opaque material layer covers the alignment mark structure, comprising:

an alignment mark region stud extending from a deep trench filled with gate material located in an alignment mark region, wherein the alignment mark region stud is formed concurrently with a formation of a circuit region stud for a vertical gate transistor in a circuit region and without requiring additional processing steps solely for the formation of the alignment mark region stud, and wherein the alignment mark region stud has a top area defined by an active area mask;

an isolation trench formed adjacent to the deep trench filled with gate material in the alignment mark region, the alignment mark region isolation trench being filled with insulating material, wherein the alignment mark region isolation trench filled with the insulating material is formed concurrently with a formation of an isolation trench filled with the insulating material that is located adjacent to the vertical gate transistor in the circuit region, and without requiring additional processing steps solely for the formation of the alignment mark region isolation trench filled with the insulating material; and

a step feature formed between the top of the insulating material in the alignment mark region isolation trench and the top of the alignment mark region stud, wherein the height of the step feature is large enough that the step feature remains visible after the opaque material layer covers the alignment mark structure.

43. The alignment mark structure of claim 42, wherein the alignment mark region is located in a kerf region of a wafer.

44. The alignment mark structure of claim 42, wherein the alignment mark region is located in the circuit region.

45. The alignment mark structure of claim 42, wherein the opaque material layer comprises a gate conductor material.